Benchmarking Planning Applications on the Qualcomm Snapdragon

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Abstract

We benchmark several space planning/scheduling applications on the Qualcomm Snapdragon 855 Handheld Development Kit (HDK), a high performance embedded processor used in many mobile phones. We are flying 2 Snapdragon HDKs onboard the International Space Station (ISS) where they are hosted by the the Spaceborne Computer-2 by Hewlett Packard Enterprise linked by USB and 12V power delivery.

We run computational benchmarks using three planner/schedulers that are used for several space missions: Multi-Mission Executive (MEXEC), Compressed Large-scale Activity Scheduling and Planning (CLASP), and M2020 Ground Scheduler (Copilot). We compare the Snapdragon performance to a performance baseline on Linux workstations. In addition, we are currently working on benchmarking the same applications on other space flight processors, such as the LEON4 Processor on the Sabertooth card, the LEON3 Processor on the Sphinx card, and the RAD750 processor.

Introduction

Flying planning and scheduling software onboard spacecraft can greatly increase the autonomy of the spacecraft, increasing science return and decreasing dependency on human operators. However, operating planning software onboard flight processors faces multiple challenges. Planning software typically requires more computing resources than traditional spacecraft flight software, specifically CPU throughput, and memory [Tran et al.2004].

In this paper we study the Qualcomm Snapdragon 855, a "system on a chip". Specifically, we study the performance of several planning algorithms, some of which have flown on previous missions. The primary metric is the runtime of the sample scenarios. These benchmarks are being run on the 855, and in the future, the LEON4 Sabertooth [Själander, Habinc, and Gaisler], the LEON3 Sphinx [Sturesson et al.2011], and the RAD750 [Berger et al.2001] as comparisons. In addition, the planner scenarios are being baselined on Spaceborne Computer-2(SBC2), a commercial super computer (high performance linux server) onboard the International Space Station(ISS) [HPE].

In addition to terrestrial benchmarking, the planning applications are being run onboard two Qualcomm Snapdragon 855 boards onboard SBC2 on the ISS. The Snapdragons are connected to SBC2 via USB and 12V power delivery. The planning applications are run on both SBC2 (under Linux), and the 855 (under Android). Many other non-planning applications, such as instrument data processing [Mirza et al.2021] and machine learning applications [Dunkel et al.2021] are also being run and benchmarked aboard SBC2 and the connected Snapdragons.

In this paper, the planning applications benchmarked are the Multi-Mission Executive (MEXEC), Compressed Large-scale Activity Scheduling and Planning (CLASP), and M2020 Ground Scheduler (Copilot).

Related Work

AI-based Planners have been flown onboard spacecraft since 1999, starting with the Remote Agent Experiment onboard Deep Space 1 (DS-1). DS-1 flew a 25 MHz radiation-hardened RAD 6000 PowerPC processor developed by IBM [rad2008]. The Remote Agent Experiment flew onboard DS-1 for 48 hours, demonstrating closed-loop, goal-based commanding onboard a spacecraft [Jónsson et al.2000].

The Autonomous Sciencecraft Experiment (ASE) flew for over 12 years from 2003-2017 on the Earth Observing One (EO-1) spacecraft. ASE used the Continuous Activity Scheduling Planning Execution and Replanning software (CASPER), an onboard planner and scheduler, performing continuous onboard (re) planning and working in concert with the Spacecraft Command Language (SCL) robust execution system. [Chien et al.2005] ASE on EO-1 flew on a Mongoose V, a radiation hardened version of the MIPS R3000, running at 12 MHz [Cressler and Mantoot2017]. Many of the flight software(FSW) concerns mentioned in [Tran et al.2004] informed software checks, flight rules, and discussions for this work. In particular, limited observability, limited memory, and limited CPU were all part of discussions relating to the Qualcomm Snapdragon and other boards.

CASPER was once again flown in space onboard the Intelligent Payload Experiment (IPEX) in 2013 for over a year. IPEX was a 1U Cubesat that flew with a 400MHz Atmel

ARM9 chip running Linux. IPEX also carried a second processor, a Gumstix Earth Storm System on a Chip (SoC). The IPEX experiment showed autonomous operations and instrument processing on multiple processors, highlighting the utility of a high performance coprocessor. [Chien et al.2016]

The ASTERIA Cubesat was a 6U satellite running F' [Bocchino et al.2018] on Linux. ASTERIA flew with a Cortex 160 Flight Computer, which contained a pair of 400 MHz PowerPC 405 processors running Real Time Linux (RTOS) [Cor]. During its third extended missions, ASTERIA ran experiments with the Multi-Mission Executive (MEXEC), a planner and scheduler built specifically for flight missions. MEXEC ran several different scenarios on ASTERIA and the ASTERIA testbed [Troesch et al.2020]. These experiments encountered many of the same FSW concerns and issues discussed in [Tran et al.2004], such as limited memory and limited CPU.

Processors

Qualcomm Snapdragon 855

The Qualcomm Snapdragon 855 is an 8 CPU core ARM system on a chip which features 4 high-efficiency "silver" cores, 3 high-performance "gold" cores, and 1 even higher performance "gold plus" core. The board also has an integrated Adreno 640 Graphics Processing Unit (GPU), a Qualcomm Hexagon 690 Digital Signal Processor (DSP), and a Neural Processing Engine (NPU) for accelerated runtime of Neural Networks [SD]. Porting the planning and execution C/C++ applications to the Snapdragon primarily involves building the application and all related libraries for the ARMv8-A architecture. All of these 3 planning applications were ported directly to the ARM cores and do not yet take advantage of the GPU, DSP, or NPU. Two out of three of the planning applications also do not yet make use of the multiple ARM cores. Further leveraging parallelization across cores or specialized GPU, DSP, and NPU coprocessors is an area of future work.

Spaceborne Computer-2

Spaceborne Computer-2 (SBC2) is a commercial, off-the-shelf supercomputer by Hewlett Packard Enterprise(HPE) with an Intel Xeon Gold 5215 Processor. The 5215 contains 10 cores, each of which can run 2 threads simultaneously, effectively giving the machine 20 cores operating at 2,500 MHz [HPE]. SBC2 has 4 NVIDIA Tesla GPUs available for computationally demanding problems that can be parallelized. In addition to the two machines onboard the ISS, there are two identical ground testbeds, each with their own Snapdragon 855 connected. For the purposes of the benchmarks, runtimes were collected on the identical ground testbed.

Sabertooth

The GR740 "Sabertooth" is a radiation-hardened system-on-a-chip with LEON4 SPARC V8 processor. The GR740 contains four 250 MHz cores and is part of the European Space Agency (ESA) standard for flight processors [Själander, Habinc, and Gaisler]. We are currently in the process of benchmarking the three planning applications on the Sabertooth. Only MEXEC has a runtime available for comparison as of now.

Planning Applications

MEXEC

The Multi-Mission Executive, MEXEC, is an integrated scheduler and executive [Verma et al.2017]. MEXEC that has flown onboard the ASTERIA cubesat [Troesch et al.2020]. MEXEC is also used in several research tasks including the Europa Lander Prototype [Wang et al.2020]. A portion of MEXEC's Timeline Library is adapted for future use on-board the Mars 2020 Perseverance Rover [Rabideau et al.2020] and is designed to run on the Perseverance Rad750 (allocated only a fraction of the CPU).

MEXEC is comprised of two separately threaded components, the planner and the executive. In addition, MEXEC requires a command dispatcher and a state database to exist, each of which also run on their own threads. However, the planner is by far the most computationally expensive component as well as the longest running. Because of this, only the planner was used for benchmarking purposes. Since an MEXEC run does not truly have a "completion" time, we measure take our metrics of the initial planning cycle as a standardized and computationally demanding benchmark.

For these benchmarks, MEXEC runs exercising test scenarios from the Europa Lander Prototype. These multi-day scenarios exercise MEXEC's planning and scheduling features such as hierarchical task planning, constraint satisfaction, and valid interval search.

Building for each of the boards involved cross-compiling the MEXEC application for that processor. In some cases it also involved implementing small changes to the way the input files were read in, the way the output files were printed, or memory reducing configuration changes. We looked at application runtime as our only metric of concern for now.

Figure 1 shows that for this CPU only, single core MEXEC planning scenario, the Snapdragon 855 is able to perform similarly to the SBC2 super computer. The 855 also performs significantly faster than the LEON4 Sabertooth. While the Sphinx and RAD750 are not yet benchmarked, we expect that they will take longer to run than any of the above.

CLASP

Compressed Large-scale Activity Scheduling and Planning, CLASP, is a long-term coverage planner for non-agile space mission coverage planning. CLASP takes in models of the spacecraft, instruments and bodies, as well as defined science "campaigns". These campaigns define the regions of a body to map, as well as geometric constraints such as illumination and distance. From this information, CLASP generates a grid representation of the body being imaged and intersects the grid points with the visibility swaths of the various instruments. Finally, CLASP uses a priority-based, greedy scheduler with Squeaky Wheel Optimization to schedule observations [Knight and Chien2006]

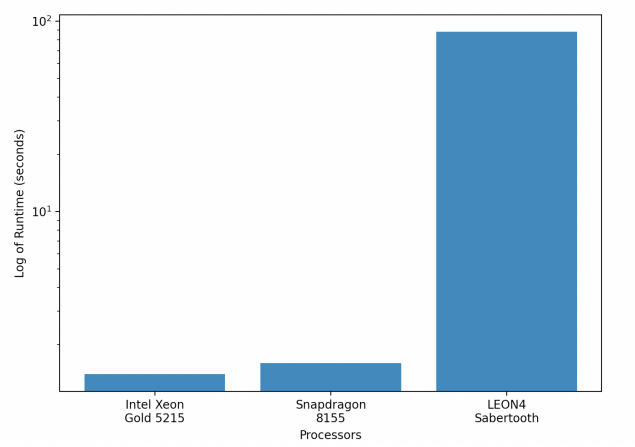

Figure 1: Runtimes of the MEXEC benchmark across various flight processors.

CLASP has been or is being used for several missions, including NISAR [Doubleday and Knight2014], ECOSTRESS [Yelamanchili et al.2019b], OCO-3 [Yelamanchili et al.2019c], and EMIT [Yelamanchili et al.2019a]. For the Snapdragon port, CLASP is running 2 years worth of 2 week runs using ECOSTRESS mission planning data from 2018 to 2020. For the purposes of comparison, the runtime of a single 2 week run is used.

The CLASP runtimes shown in Figure 2 are for a single threaded CPU implementation. The CLASP scenario is longer running and more computationally complex than MEXEC, so the difference between the 855 and SBC2 is more stark. We expect that both runtimes would greatly outperform the LEON processors or the RAD750. These benchmarks are being collected now. The CLASP planning problem in particular performs a large amount of ray tracing in order to compute when targets are visible during the spacecraft orbit. As this type of ray tracing is exactly what GPU co processors are designed to efficiently perform in a massively parallel fashion, it is believed that CLASP could show dramatically improved performance by leveraging the GPU on either Snapdragon or SBC2.

M2020 Copilot

The M2020 Copilot ground scheduler is currently in use on the ground scheduling wake/sleep [Chi, S.Chien, and Agrawal2020] and preheats for M2020 operations. Challenges in M2020 scheduling include complex wake/sleep constraints, preheat constraints, variability in in execution [Chi et al.2019], and complex operations handover handling. The M2020 Copilot ground scheduler uses the same scheduling algorithms as the M2020 Onboard scheduler [Rabideau et al.2020]. The Snapdragon test is about 800 M2020 planning problems that are designed random variations of 7 base plans or "sol types". These plans vary aspects such as execution duration(s), incoming and outgoing energy state, and alternative action options.

Copilot was first ported to run each sol type in serial, running single threaded. Since the large problem was already split into 800+ iterations, we were able to parallelize Copilot in particular. Runtimes are compared for the serial version in Figure 3. For the parallelized version in Figure 4, SBC2 was benchmarked with an 8 core case, to match the 855's 8 cores, as well as a full 20 core case. All other future benchmarks, the LEON3, LEON4, and RAD750, have four or fewer cores, and would likely take longer to run on each core as well.

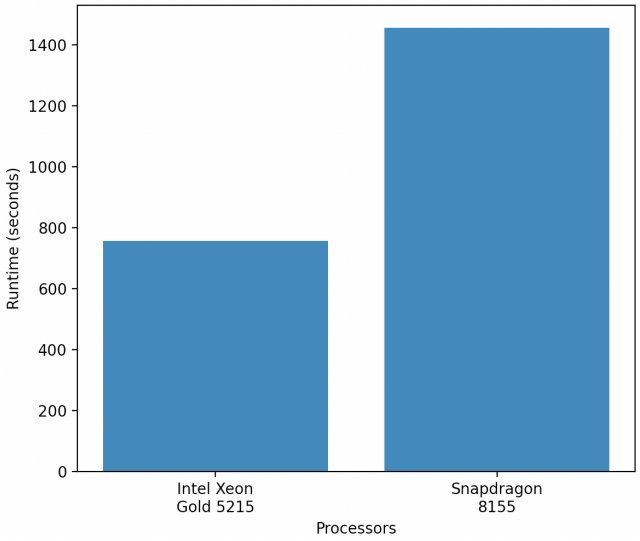

Figure 2: Runtimes of the CLASP benchmark across various flight processors.

Future Work

In addition to comparing the performance of the Snapdragon 855 board to the SBC2 Linux machine, we plan to compare the performance to other space flight processors. All three planning algorithms are currently being ported for the LEON4 Sabertooth, the LEON3 Sphinx, and RAD 750. Some preliminary analysis and the specifications of the board imply that the Snapdragon 855 will significantly outperform all of the traditional flight CPUs.

Presently, only a single ARM core is used on the Snapdragon to run MEXEC and CLASP. Copilot can run its 800+ iterations across all eight cores, however still only on the ARM CPU. The Snapdragon 855 features an Adreno 640 GPU, a Hexagon 960 DSP, and a Neural Processing engine, none of which are being used by any of the planning applications. In particular, CLASP could take major advantage of the GPU for its visibility computation. Both CLASP and MEXEC could see major speedups if parallelized across multiple cores as well.

There are many other applications being ported, benchmarked, and run on the ISS Snapdragons. Many instrument processing algorithms, such as Hyperspectral Compression [Hernandez-Cabronero et al.2021] and Synthetic Aperture Radar (SAR) image processing [Hawkins and Tung2019] are being run on the Snapdragons CPU and GPU. In ad-

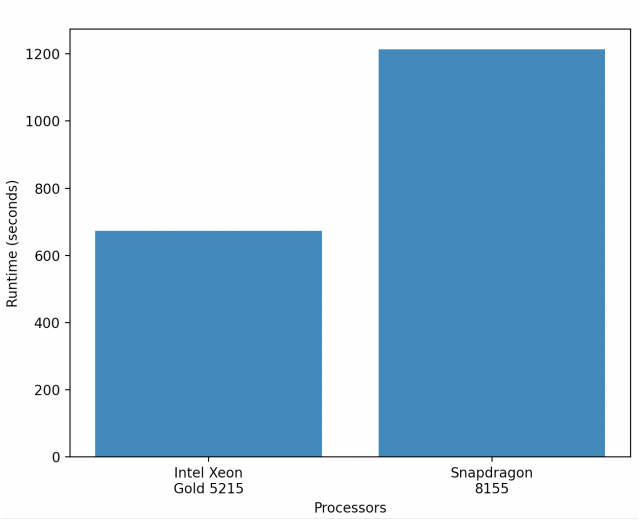

Figure 3: Runtimes of the Copilot benchmark across various flight processors run over many sol types serially.

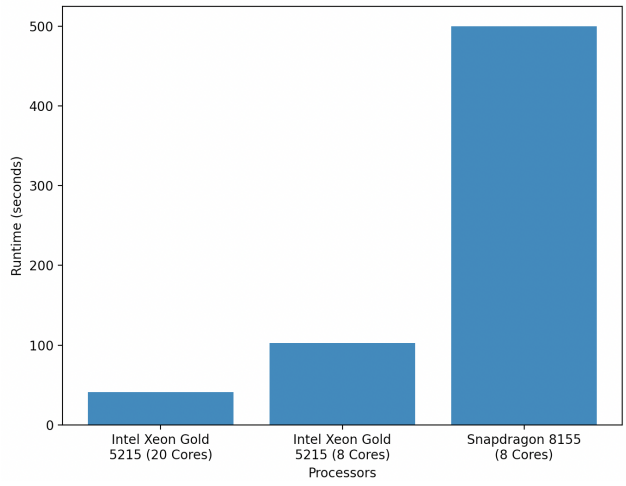

Figure 4: Runtimes of the Copilot benchmark across various flight processors run over many sol types in parallel.

dition, many Machine Learning applications are being run on the CPU, GPU, or NPU. These classifiers include neural networks trained on Mars imagery from the Reconnaissance Orbiter, Curiosity rover, and others [Dunkel et al.2021]. Other more general benchmarks, such as matrix multiplication and Fourier transforms, are being run on the CPU, GPU and the DSP. The Snapdragon 855 is also being benchmarked on its radiation hardness.

Conclusion

In this paper we described preliminary efforts evaluating the Qualcomm Snapdragon 855 processor as a flight processor or coproccessor for planning applications onboard space missions. We measure initial runtime benchmarks of three planning applications, MEXEC, CLASP, and Copilot on the 855. These runtimes are compared to the runtimes of the same scenarios with the same applications on different processors, varying from conventional flight processors to high performance Linux compute servers. We show that the Qualcom Snapdragon out-performs other traditional flight computers benchmarked, showing performance comparable to a linux desktop machine, as measured by run time on benchmark problems. We also fly these algorithms on a snapdragon onboard the ISS as a flight demonstration. Flight demonstration and benchmarking of these planning algorithms is intended to facilitate future flight of these capabilities to enable future single and networked autonomous spacecraft missions.

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